CS-99-210

IN THE CLAIMS

Please amend Claim 1 as follows:

1. (Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a metal layer overlying said semiconductor substrate;

etching through said metal layer to form connective lines;

thereafter etching partially through said metal layer to form vias using a timed etch;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

Please cancel Claim 4.

Please amend Claim 9 as follows:

9. (Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, and said first metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias using a timed etch;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said